REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 47, 55, 65, and 69 are currently being amended.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 47-78 are now pending in this application.

Drawings

In section 2 of the Office Action, the Examiner objected to the drawings as failing to comply with 37 CFR § 1.84(p)(4) because reference characters 720 and 705 have both been used to designate the same element in Figure 8, and the numerical references 730 and 710 designate the same part in Figure 8. The Examiner has requested a proposed drawing correction.

With regard to the objection to Figure 8, Applicants respectfully disagree. Applicants respectfully submit that the drawings appear to be clear and reference characters 720 and 705 are clearly described in the specification. Applicant refers the Examiner to the second paragraph starting on page 10 of the original specification. What is disclosed is a "substrate 705 (e.g., silicon, gallium arsenide, etc.) may be overlaid with second material 710 (e.g., doped silicon, doped gallium arsenide, other non-doped materials, etc.) forming a plurality of gates patterned in second material 710. Further, the device may include a plurality of laser light sources 720 having a first layer 730 (e.g., semiconductor) overlaid with a second layer 740 (e.g., semiconductor) and having a doped junction 750 therebetween." Accordingly, the arrow tipped lead line associated

with 720 is pointing to a laser light source which comprises the three layers 730, 740 and 750, whereas reference numeral 705 is indicating the substrate along the bottom of the device shown in Fig. 8. Accordingly, Applicants respectfully request the withdrawal of the objection to characters 720 and 705 being used to designate the same elements in Fig. 8. It is clear that the elements to which each reference number is directed is clear.

The Examiner also objected to the drawings because reference numerals 730 and 710 designate the same part in Fig. 8. Applicants respectfully request that the Examiner withdraw the objection because it is clear from the specification, again in the second paragraph starting on page 10 of the original specification, that there is a patterned gate structure 710 and there is a substrate 705. These two layers are clearly different layers in Fig. 8 and Applicants do not understand how it could be interpreted in any other way. The combination of the specification in Fig. 8 make clear that the reference numerals 730 and 710 do not designate the same part. Accordingly, Applicants respectfully request the withdrawal of the objection.

Claim Rejections – 35 U.S.C. § 112

In section 4 of the Office Action, the Examiner rejected Claims 47-78 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The Examiner indicated that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor at the time the application was filed had possession of the claimed invention. The Examiner indicated that:

> The specification and the claims fail to teach what is considered to be an '*interference line*'. It is known that when two coherent light beams intercept with each other, they interfere with each other. The wavefront of the coherent light beams are generally spread out and the wavefronts for the coherent light beams will intercept at many different locations and different directions, (please see the wavefront demonstration in Figures 2-5 in particular in this application), and since an interference region is claimed for the coherent light beams to intercept, it is therefore not possible to have just *an* interference line and event to determine *an* interference line.

Applicants respectfully submit that Claims 47 , 55 and 69 have been amended for clarity. Applicants have recited in Claim 47 "the interference region comprises the second material, the first and second optical inputs are spaced apart and the output is positioned along a chosen line, of many lines, along which destructive interference occurs when the light input at the second input is on." Also, Claim 55 has been amended to recite "an interference region coupled to at least two of the optical conduits that are configured to receive optical input signals, the interference is caused along a predetermined axis in the interference region and along other axes in the interference region." Similarly, claim 69 has been amended to recite "the location of a chosen line of many lines, along which destructive interference to wavefronts of light from the optical input signals entering the interference region is predicted based on the distance between . . ." Accordingly, Applicants have clarified that there are more than one line or axis along which destructive interference will occur in the interference region as depicted in Figs. 2-5. However, Applicants have also identified that there is a chosen line or a predetermined axis along which the output of the optical logic circuit is aligned. With regard to independent Claim 65, Applicants respectfully submit that "an interference line" is not recited and thus the Examiner's rejection under 35 U.S.C. § 112 does not apply. Accordingly, Applicants respectfully request the withdrawal of the claim rejections under 35 U.S.C. § 112, first paragraph, of Claims 47-78.

In section 5 of the Office Action, the Examiner rejected Claims 68, 73, and 77 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Examiner indicated that

> The specification and the claims fail to teach how could 'the interference region is configured to cause substantially no light exiting the interference region output when both light and no light is provided to both of first and second coherent light inputs', as recited in amended claim 73. It is not clear how could this be possible that no light exit from the interference region when light either enters or not enters the first and second optical paths. In particular, the claims are drawn to an optical logic circuit wherein interference between the light entering the interference region is *essential* requirement for the operation of the optical logic.
>
> The specification and the claims also fail to each how could the optical logic circuit provides both the NOT and NOT AND logical functions, as recited in claims 68 and 77. The applicant is respectfully noted that page 6 of specification only discloses that the NOT AND (NAND) gate is used to construct a NOT gate. The specification does not give positive support for the logic function to be BOTH the NOT and NOT AND gates.

With regard to Claims 68 and 77, Applicants respectfully disagree with the Examiner. The Examiner says that the specification fails to teach how could the optical logic circuit provide both the NOT and NOT AND logical functions. Applicants respectfully submit that that is not what is recited in the claims. What is recited in the claims is that the Boolean logic function is configured of NOT gates and NOT AND gates. Accordingly, a Boolean logic function is built from the fundamental building blocks of NOT gates and NOT AND logical functions. It is not stated that the optical logic circuit provides both NOT and NOT AND gates. For example, Applicants refer the Examiner to Figure 4 and correspondingly, page 7, lines 11-24. These portions of the specification describe how an AND gate which is a Boolean logic function is configured of a NOT gate and a NOT AND gate by combining the two. Accordingly, the Examiner's rejection under 35 U.S.C.. § 112, first paragraph, is requested to be withdrawn

because it is clear from the specification and the figures that a Boolean logic function may be configured of NOT gates and NOT AND gates.

With regard to Claim 73, the Examiner indicated that it is not clear how no light exits from the interference region when light either enters or not enters the first and second optical paths. Applicants refer the Examiner to Table IV on page 8 and also provide the Examiner that this is the essence of an exclusive (XOR) gate 500 as depicted in Fig. 5. When light is provided to both inputs A and B, destructive interference is caused along line 530 and substantially no light is provided through output 520. Similarly, when no light is provided to input A and input B, then no light is provided through output 520. However, if light is provided to input A and no light is provided to input B, then there will be light provided through output 520. Similarly, if light is provided to input B and no light is provided to input B and no light is provided through input A, then light will be provided through output 520. Accordingly, Applicants respectfully submit that the specification teaches the subject matter recited in Claim 73. Accordingly, Applicants respectfully request that the rejection under 35 U.S.C. § 112, first paragraph, of Claim 73 be withdrawn.

Claim Rejections – 35 U.S.C. § 103

In section 7 of the Office Action, the Examiner rejected Claims 47-58 and 63-78 under 35 U.S.C. § 103(a) as being unpatentable over the patent issued to Usagawa et al. (U.S. Patent No. 5,233,205). With regard to independent Claim 47, Applicants have recited "the interference region comprises the second material and is uninterrupted by any other material within the interference region, the first and second optical inputs are spaced apart and the output is positioned along a chosen line, of many lines, along which destructive interference occurs when the light input at the second input is on." The Applicants respectfully submit that the structure recited by Applicants differs from the structure of Usagawa et al. in that the interference region of Applicant's invention is uninterrupted by another material within the interference region, thus the structures are more easily manufactured. For example, Figure 1D shows a barrier 2 within the interference region. As recited in independent Claim 47, the interference region is

uninterrupted by any other material which is a different structure than what is depicted in Figure 1D of Usagawa et al. in which a reference input is constantly on.

Applicants respectfully submit that it is disclosed in Figure 1E of Usagawa et al. an uninterrupted interference region, however the uninterrupted interference region 1 is not combined with a constant coherent light input from a light source. Accordingly, the combination of claim limitations recited in independent Claim 47 are not disclosed, taught or suggested by Usagawa et al. Further, if one examines the use of the uninterrupted interference region of Fig. 1E in Usagawa et al., it is disclosed that the output may have potentially three different intensities, a low or off value when X1 and X2 are not on, a medium value when either of X1 or X2 is on, and a high value when both X1 and X2 are on. Accordingly, the output 20 is not aligned with a line of destructive interference as recited by Applicants because, if it were, there would be only two output intensities as in Applicants advantageous design. Further, the outputs are not substantially on or substantially off, that is the outputs of Usagawa et al. of Fig. 1E have three different possible values. Accordingly, the sensor 20 must be more complex than the sensors used for Applicant's invention. Thus, Applicants respectfully submit that Claim 47 is not obvious under Usagawa et al. because the combination of claim limitations is not taught or suggested by Usagawa et al. and does not provide the same results as Applicant's invention.

Further, the Examiner has indicated some similarities between the quantum wave circuit described by Usagawa et al. and the optical logic circuit recited by Applicants. Applicants however disagree with the Examiner's interpretation. The optical logic circuit is based on propagation of photons through the material and the destructive interference of wavefronts of photons propagating through the material not through a propagation of electrons and holes through a material. The Examiner also states that the quantum well structures require incident light to excite the electron and hole carriers. However, there are ways in which the electron hole carriers may be induced as opposed to light and the inducement of the electron hole carriers by light is not described, taught, or suggested by Usagawa et al. Further, although what is described by Usagawa et al. is wave-like behavior of electron waves, light is not propagated through the

material causing destructive interference as recited in the claims. Accordingly, the equivalence of an electron wave and a light wave has not been established by Usagawa et al. Thus, for the additional reasons, independent Claim 47 and its dependent claims are allowable.

With regard to independent Claim 55, independent Claim 55 is allowable for substantially the same reasons as independent Claim 47.

With regard to independent Claim 65, independent Claim 65 is allowable for substantially the same reasons as independent Claim 47.

With regard to independent Claim 69, independent Claim 69 is allowable for substantially the same reasons as independent Claim 47.

Applicants respectfully submit that because Claims 47, 55, 65, and 69, as amended, are allowable, all of Claims 47-78 which include claims depending from the amended independent claims are also allowable.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

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By _____

FOLEY & LARDNER LLP
Customer Number: 26371
Telephone: (414) 297-5730
Facsimile: (414) 297-4900

Alistair K. Chan
Attorney for Applicant
Registration No. 44,603